

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S
INFORMATION DISCLOSURE STATEMENT

SERIAL NO. **Not Assigned**

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REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

MT	.	A. Yagishita et al.; "High Performance Metal Gate MOSFETs Fabricated by CMP for 0.1 μ m Regime"; 0-7803-4774-9/98, 1998 IEEE; IEDM 98-785; pgs. 29.3.1 - 29.3.4
MT	.	T. Matsuki et al.; "Cu/Poly-Si Damascene Gate Structured MOSFET with Ta and TaN Staked Barrier"; 0-7803-5410-9/99, 1999 IEEE; IEDM 99-261; pgs. 10.6.1 - 10.6.4
MT		A. Hiroki et al.; "A High Performance .01 μ m MOSFET with Asymmetric Channel Profile"; 0-7803-2700-4, 1995 IEEE; IEDM 95-439; pgs. 17.7.1 - 17.7.3
MT	.	A. Yagishita et al.; "High Performance Damascene Metal Gate MOSFETs for 0.1 μ m Regime"; 0018-9383/00, 2000 IEEE Transaction on Electron Devices, Vol. 47, No. 5; pgs. 1028-1034

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